a microcontroller

a ROM memory for program storage;

a RAM memory for program execution and to maintain a set of command and attribute registers used by the microcontroller to manage the data transfer operation in and out of a plurality of flash memory;

a buffer manager for temporarily storing data to be transferred to and from flash memory;

a flash memory sequencer for controlling the transfer of a data to and from flash memory that has been received from the buffer manager; and

a data bus couple to the set of operative components that include the microcontroller, the PCMCIA-ATA flash memory interface, the IDE interface, the ROM memory, the RAM memory and the buffer manager.

2. (currently amended) ~~The compact flash controller as recited in claim 1, wherein~~

A compact flash memory controller for controlling transfer of data between flash memory and a host device comprising:

a PCMCIA-ATA flash memory interface;

an IDE interface;

a microcontroller

a ROM memory for program storage;

a RAM memory for program execution and to maintain a set of command and attribute registers used by the microcontroller to manage the data transfer operation in and out of a plurality of flash memory;

a buffer manager for temporarily storing data to be transferred to and from flash memory, the buffer manager includesing an integrated data interface ~~that is a~~ attached to the flash memory sequencer so that data segments or sectors can be moved to and from the flash memory sequencer;

a flash memory sequencer for controlling the transfer of a data to and from flash memory that has been received from the buffer manager; and

a data bus couple to the set of operative components that include the microcontroller, the PCMCIA-ATA flash memory interface, the IDE interface, the ROM memory, the RAM memory and the buffer manager.

3. (original) The compact flash controller as recited in claim 2, wherein the buffer manager further comprises an integrated data buffer to receive and store data as a least sixteen bit format.

4. (original) The compact flash controller as recited in claim 2, wherein the integrated data buffer is at least 512 kilobyte in size.

5. (currently amended) The compact flash controller as recited in claim 2 ~~1~~, wherein the data bus transports data, addresses and commands between the operative components of the controller and the host device.

6. (currently amended) The compact flash controller as recited in claim 2 ~~1~~, said flash memory sequencer comprises a counter, a sequencer RAM which stores instructions at an address which is indicated by said counter, an instruction decoder coupled with said sequencer RAM for decoding a instruction so that a decoded micro order is sent to a flash memory chip through said data bus, and a decision circuit which adjusts content of said counter depending upon an output of said AND circuit.

7. (currently amended) The compact flash controller as recited in claim 2 ~~1~~, wherein the integrated data interface attached to the buffer manager is directly interfaced to the flash memory sequencer where data from the buffer can move from a buffer location to the flash memory sequence, in parallel and without program intervention.

8. (currently amended) The compact flash controller as recited in claim 2 ~~1~~, wherein the compact flash controller can access a plurality of flash memory modules.

9. (original) The compact flash controller as recited in claim 8, wherein the flash memory modules are grouped in a two module set, one that stores odd bit data segments or sectors and the other that stores even bit data segments or sectors.

10. (original) The compact flash controller as recited in claim 8, wherein each flash memory module have a plurality of data and address elements that are least 8 bits wide.

11. (withdrawn) A flash memory system coupled with a host device comprising:

a flash memory, and

a compact flash controller for controlling data transfers between flash memory and a host device, where the compact flash controller comprises:

a PCMCIA-ATA flash memory interface;

an IDE interface;

a microcontroller

a ROM memory for program storage;

a RAM memory for program execution and to maintain a set of command and attribute registers used by the microcontroller to manage the data transfer operation in and out of a plurality of flash memory;

a buffer manager for temporarily storing data to be transferred to and from flash memory;

a flash memory sequencer for controlling the transfer of a data to and from flash memory that has been received from the buffer manager; and

a data bus couple to the set of operative components that include the microcontroller, the PCMCIA-ATA flash memory interface, the IDE interface, the ROM memory, the RAM memory and the buffer manager.

12. (withdrawn) The flash memory system as recited in claim 11, wherein the compact flash controller accesses a plurality of flash memory modules.

13. (original) A flash memory system coupled with a host device comprising:

a flash memory, and

a compact flash controller for controlling data transfers between flash memory and a host device, where the compact flash controller includes:

a PCMCIA-ATA flash memory interface;

an IDE interface;

a microcontroller

a ROM memory for program storage;

a RAM memory for program execution and to maintain a set of command and attribute registers used by the microcontroller to manage the data transfer operation in and out of a plurality of flash memory;

a buffer manager for temporarily storing data to be transferred to and from flash memory;

a flash memory sequencer for controlling the transfer of a data to and from flash memory that has been received from the buffer manager; and

a data bus couple to the set of operative components that include the microcontroller, the PCMCIA-ATA flash memory interface, the IDE interface, the ROM memory, the RAM memory and the buffer manager; and

access to a plurality of flash memory modules and the flash memory modules are grouped in a two module set, one that stores odd bit data segments or sectors and the other that stores even bit data segments or sectors ~~The flash memory system as recited in claim 12, wherein~~.

14. (original) The flash memory system as recited in claim 13, wherein each flash memory module have a plurality of data and address elements that are least 8 bits wide.

15. (withdrawn) A method of controlling the transfer of data between flash memory and a host device performed by a compact flash controller comprising the steps of:

receiving power up sequence from host device;

initializing controller, a plurality of flash memory modules as well as other internal components;

reading an incoming OE/ATSEL signal that indicates which interface specification is to be used for to transfer data, address information and control signals to and from the host device;

detecting that there is a command to be processed;

selecting the command specified by a plurality of command parameters from at least one register found in an attribute memory of the compact flash controller; and

executing the command.

16. (withdrawn) The method as recited in claim 15, wherein if the received state of the OE/ATSEI signal is high then a PCMCIA/ATA interface is selected to receive as well as transfer of data, address information between flash memory and a host device.

17. ((withdrawn) The method as recited in claim 15, wherein if the received state of the OE/ATSEI signal is low then a true IDE interface is selected to receive as well as transfer of data, address information between flash memory and a host device.

18. ((withdrawn) The method as recited in claim 15, wherein the command specified by the plurality of command parameters writes data and address content

received from the host device to at least one odd bit partition and at least one even bit partition of flash memory.

19. (withdrawn) The method as recited in claim 15, wherein the command specified by the plurality of command parameters reads data and address content from at least one odd bit partition and at least one even bit partition of flash memory that is transferred back to the host device.

20. ((withdrawn) The method as recited in claim 15, wherein the command specified by the plurality of command parameters is a command that controls the operation of the compact flash but does not perform a data transfer between the host device and the flash memory.

21. (withdrawn) The method as recited in claim 15, wherein after the compact flash controller has executed the specified command, the compact flash controller stands idle waiting a predetermined time period for the next command to execute.

22. (withdrawn) The method as recited in claim 15, wherein after if the a predetermined time period elapses, the compact flash controller suspends any operative activity and waits until a request to execute a new command has been detected.

* * * R*E*M*A*R*K*S * * *

Applicants herewith submit this Response A in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicants respectfully request reconsideration of the above-identified application in view of the amendments to the specification, claims and drawings, and the remarks set forth below.